The basic concepts and the related abbreviations of MOSFET

Teimuraz Mchedlidze

Institut für Angewandte Physik
Technische Universität Bergakademie Freiberg,
Freiberg, Germany

International School and Conference on Functional Materials for Modern Technologies

ISCFMMT 2022

Batumi Shota Rustaveli State University, Batumi, Georgia October 1-7 2022

Preparation for the presentation:

“Characterization methods for FD SOI HKMG stacks”

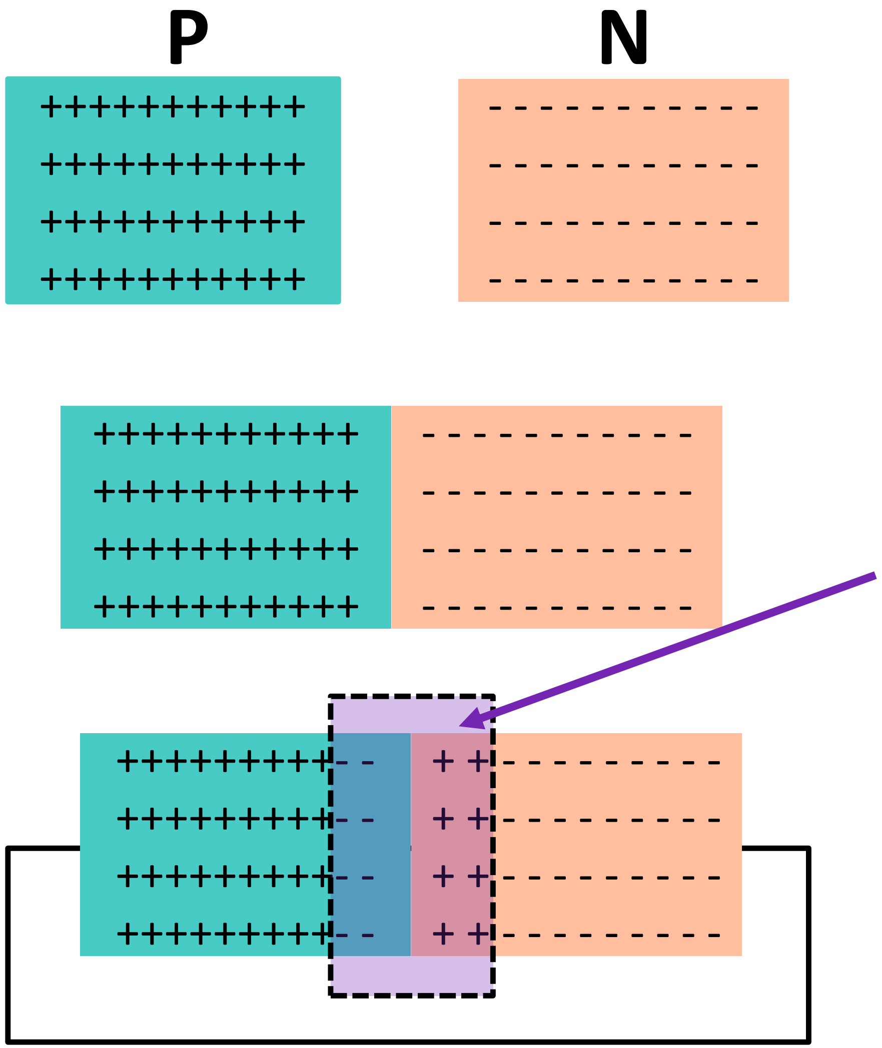
1. FD SOI ?
2. HKMG Stack ?
3. MOSFET, I_dV_g , V_{th} and STS (SS) ?

Question for the students: Is here somebody familiar with the above abbreviations to help me with the explanations?

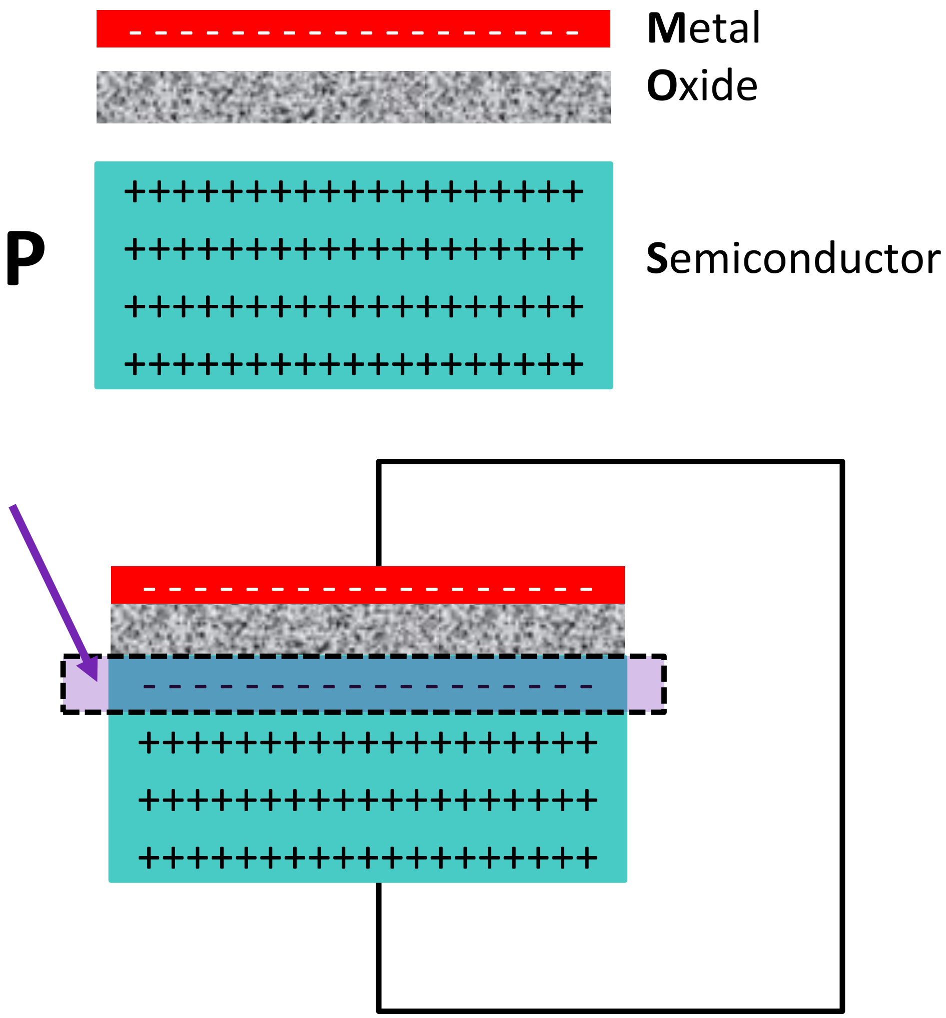
▶ L.R Linares and J. Yan (2013)
📖 A.S. Sedra and K.C. Smith, “Microelectronic Cirquits”, 6th edition (2009)

FD SOI – fully depleted SOI

PN-junction



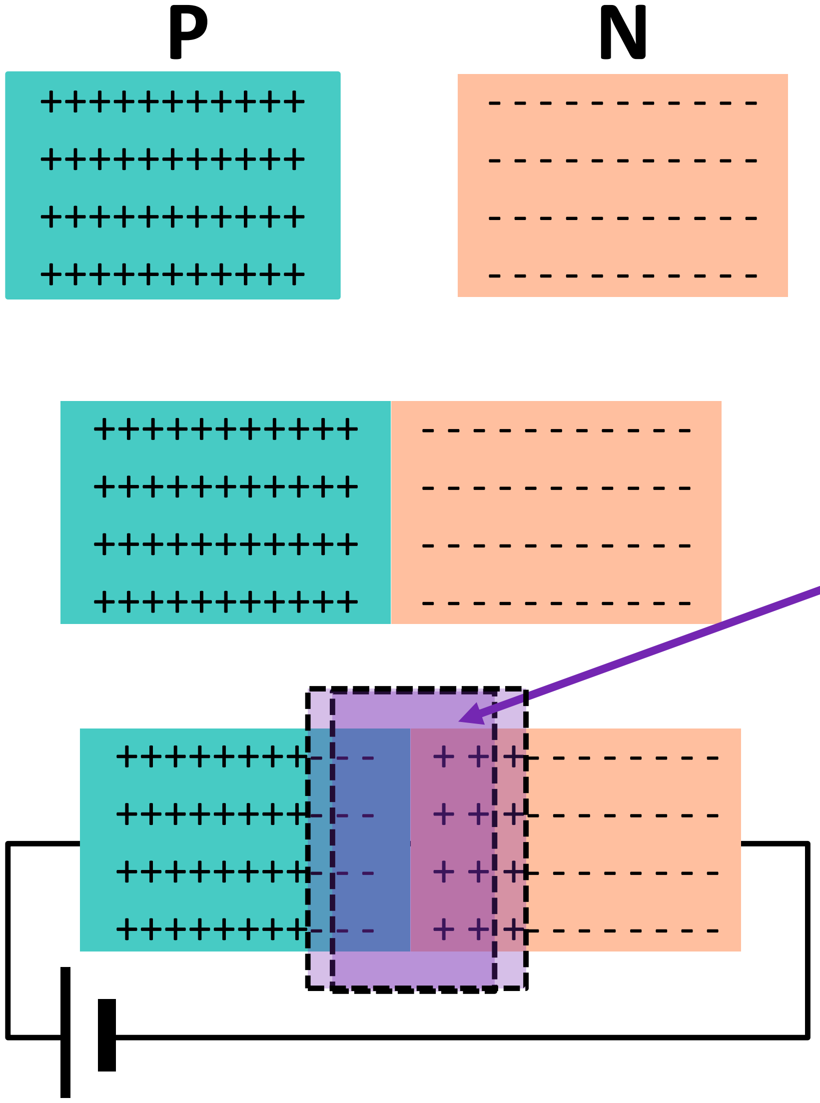
MOS capacitor



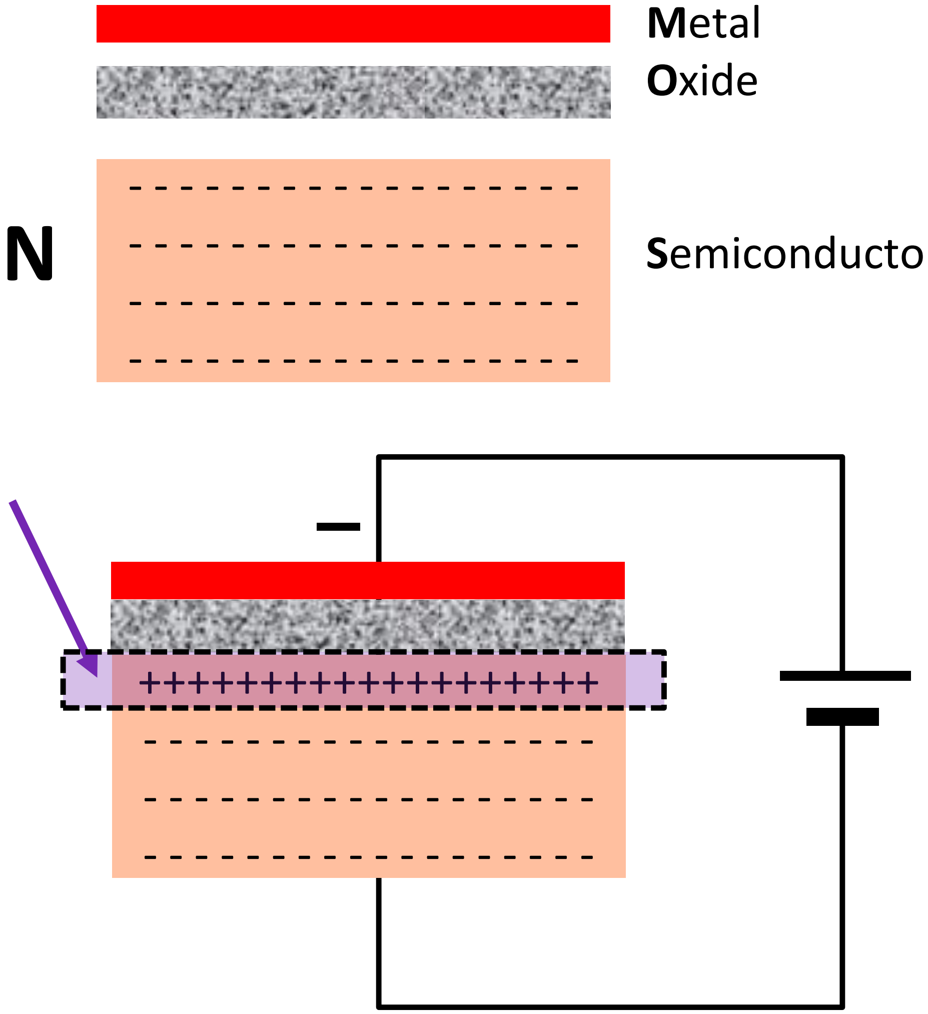
Depletion zone:
no free charges

FD SOI – fully depleted SOI

PN-junction

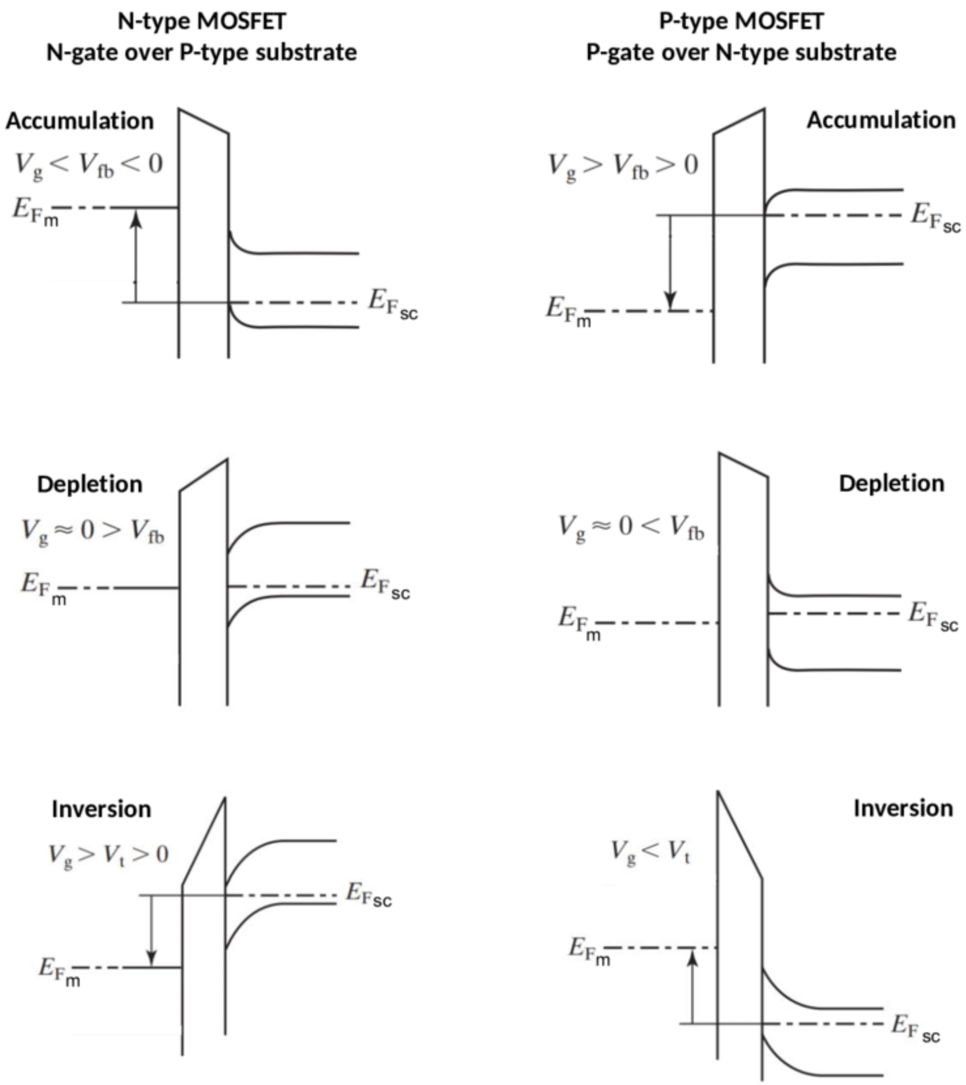


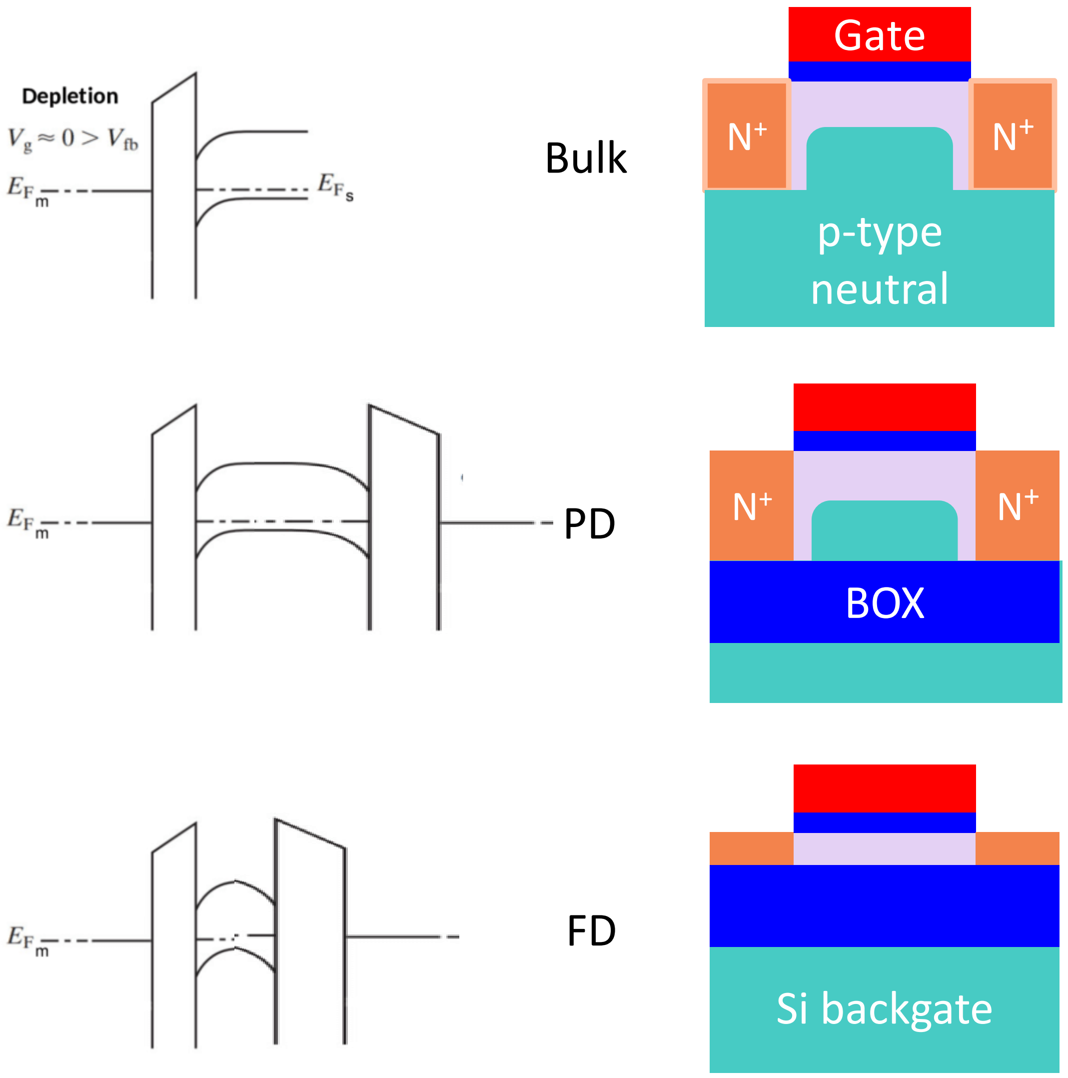
MOS capacitor



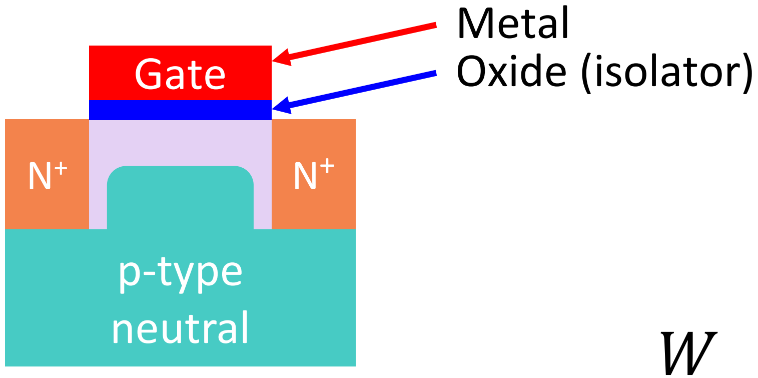
Depletion zone:
no free charges

FD SOI – fully depleted SOI





High-K metal gate stack

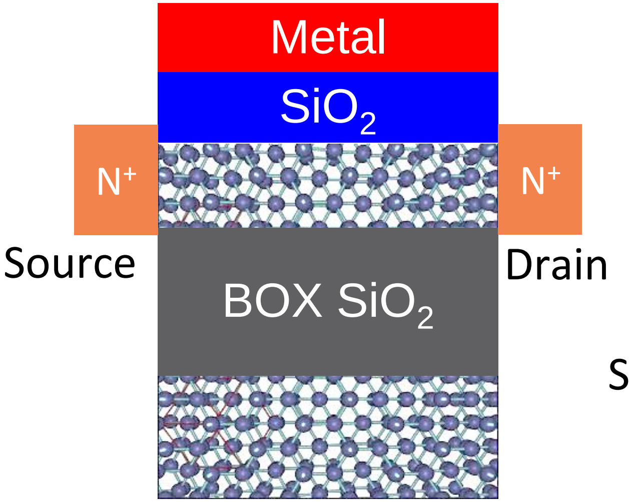


$$\boxed{C} = \boxed{\frac{k\varepsilon_0 A}{t_{OX}}}$$

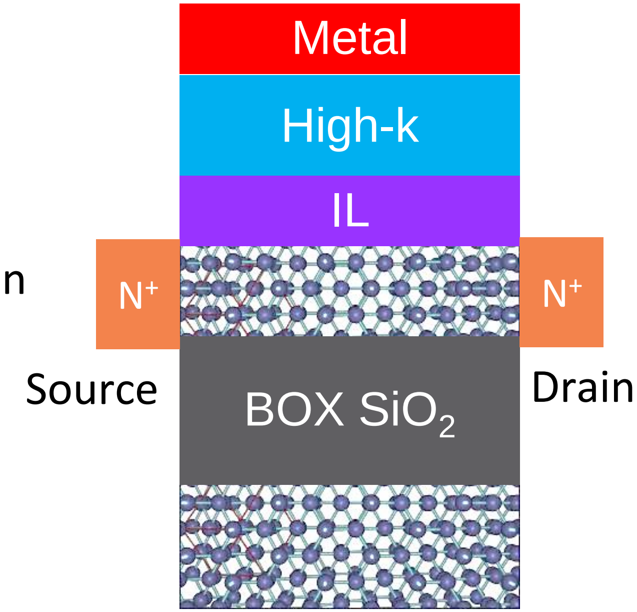
- *A* is the capacitor area
- *κ* is the relative dielectric constant of the material (3.9 for silicon dioxide)
- ε_0 is the permittivity of free space
- *t* is the thickness of the capacitor oxide insulator

$$I_{D,sat} = \frac{W}{L}\mu \boxed{C_{inv}} \frac{(V_G - V_{th})^2}{2}$$

- *W, L* are the width and the length of the transistor channel
- *μ* is the channel carrier mobility
- C_{inv} is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state
- V_G is the voltage applied to the transistor gate
- V_{th} is the threshold voltage



1.2 nm SiO_2:
Capacitance = 1×
Leakage Current = 1×

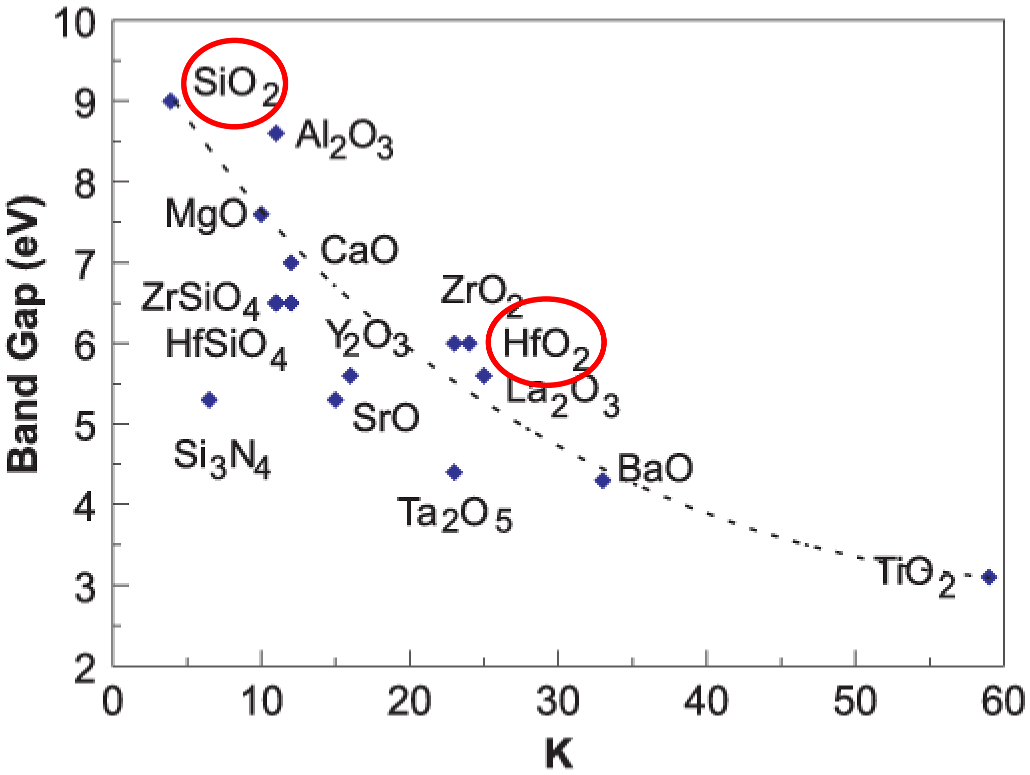


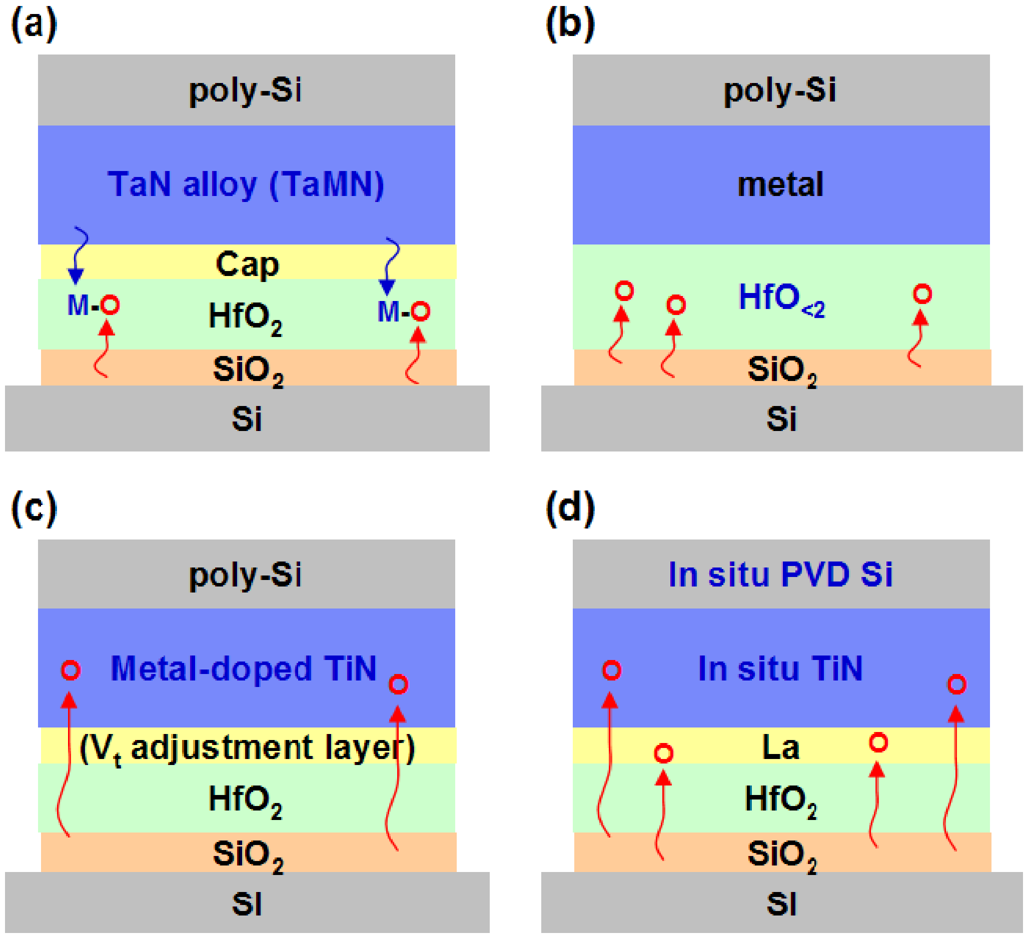
3 nm high-k+IL:
Capacitance = 1.6×
Leakage Current = 0.01×

Question for the students: So what is the effective *k* for the right picture?

Answer: *k*=14

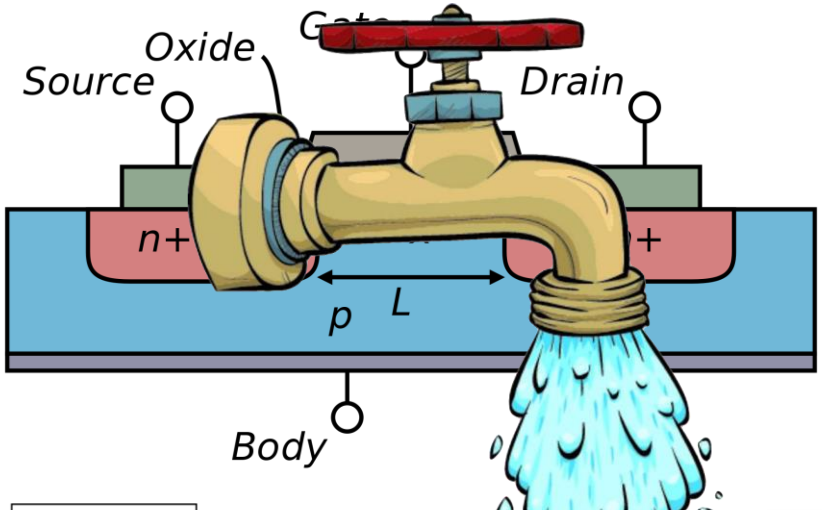
High-K metal gate stack

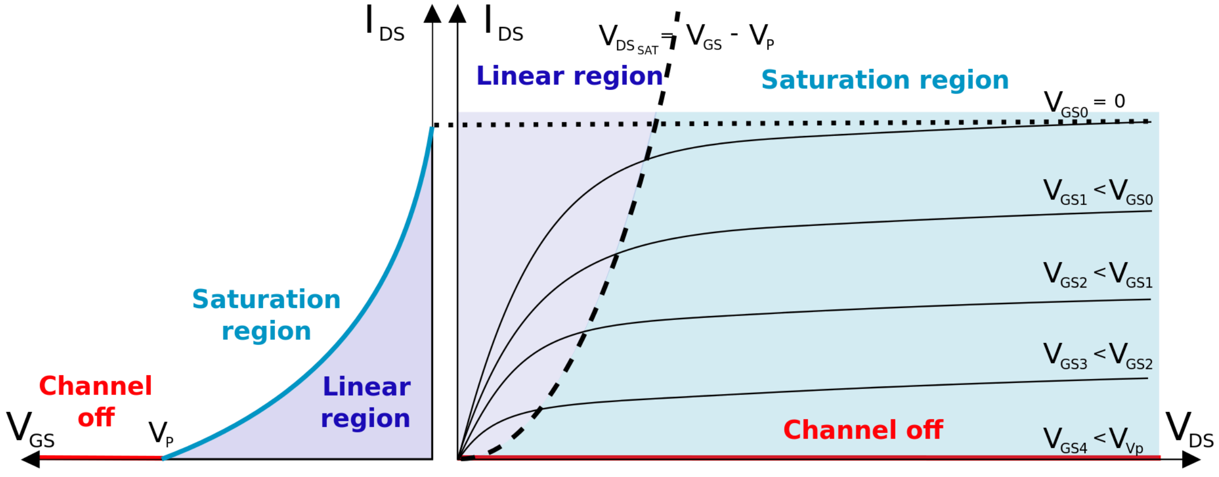




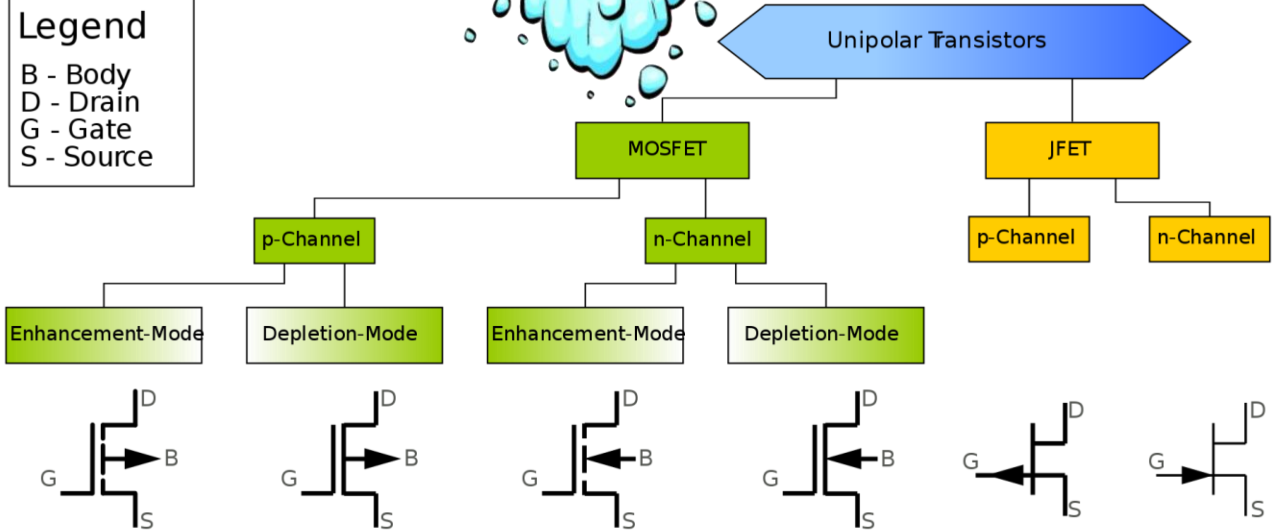
K. Yim, et al., NPG Asia Materials, 2017, 7, 190

MOSFET and parameters





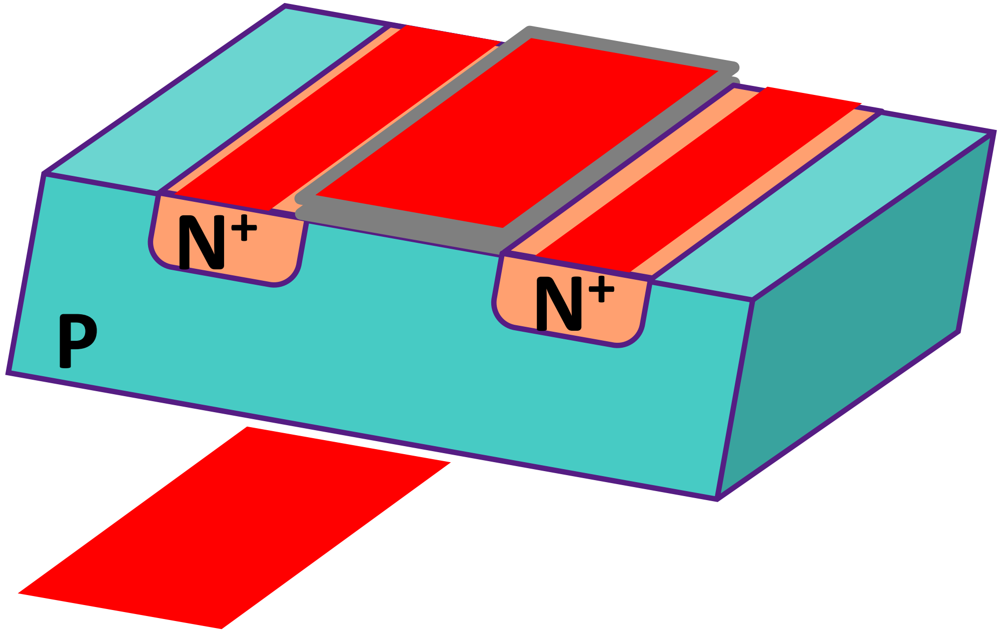
Legend
B - Body
D - Drain
G - Gate
S - Source

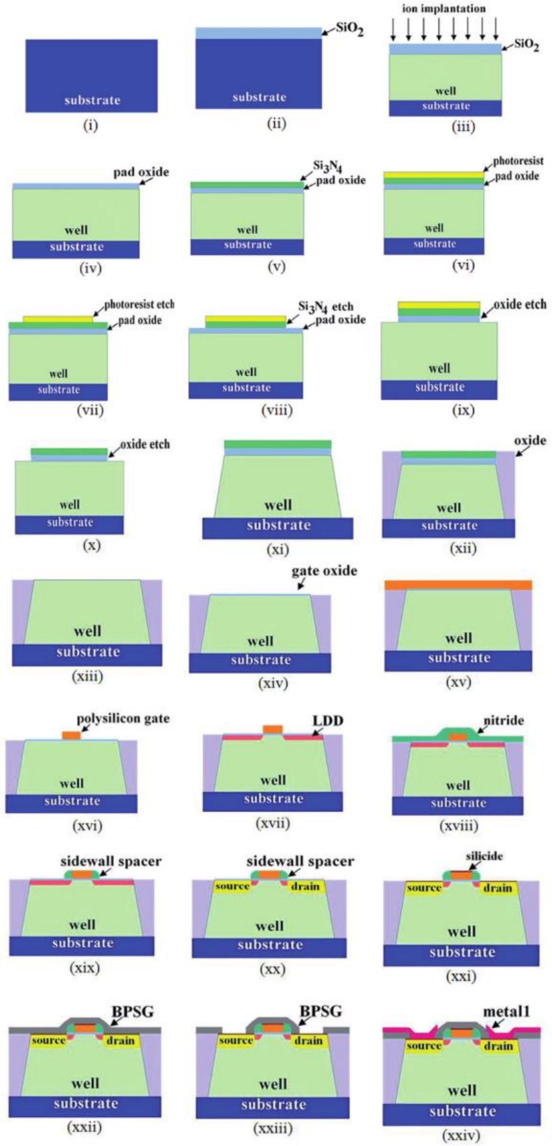


By Tech2077 - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=65081300

By JFET_n-channel.svg: Phirosiberiaderivative work: Phirosiberia (talk) - JFET_n-channel.svg, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=7042107

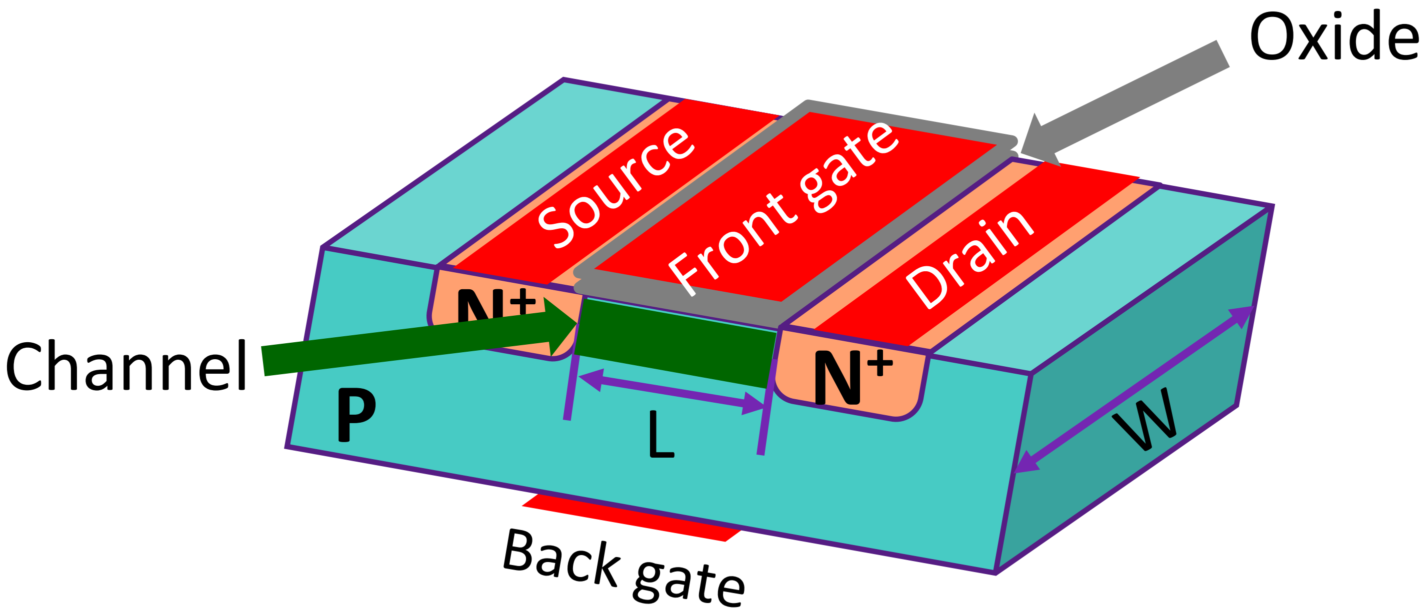
FET construction



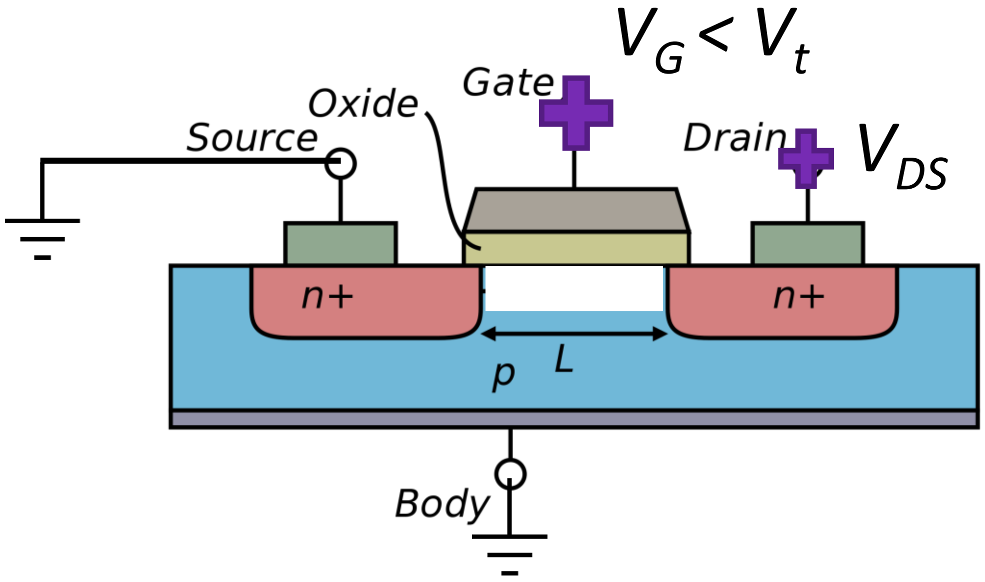


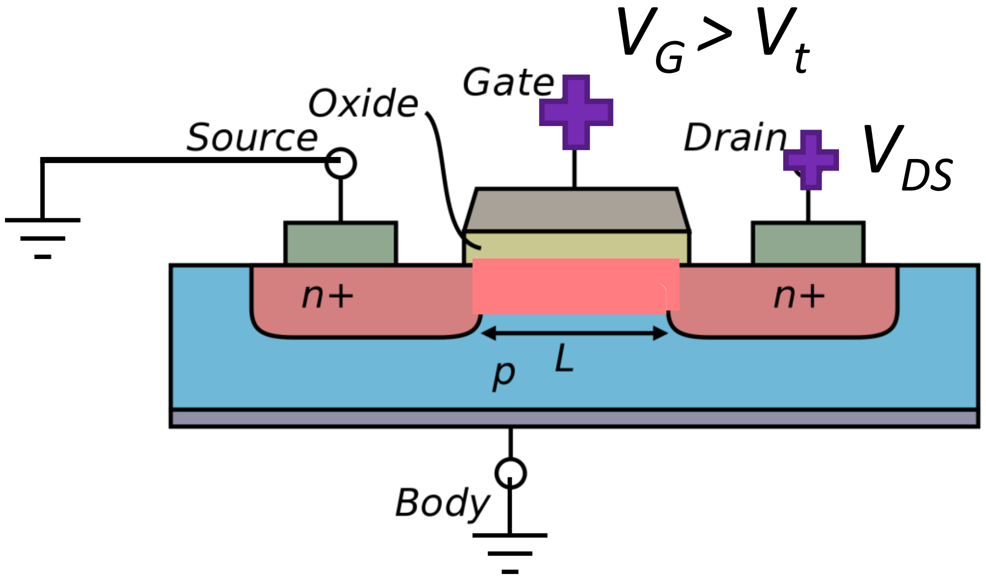
K.H. Yeap, M.M. Isa and S. H. Loh, (2020)
DOI: 10.5772/intechopen.92818

FET construction

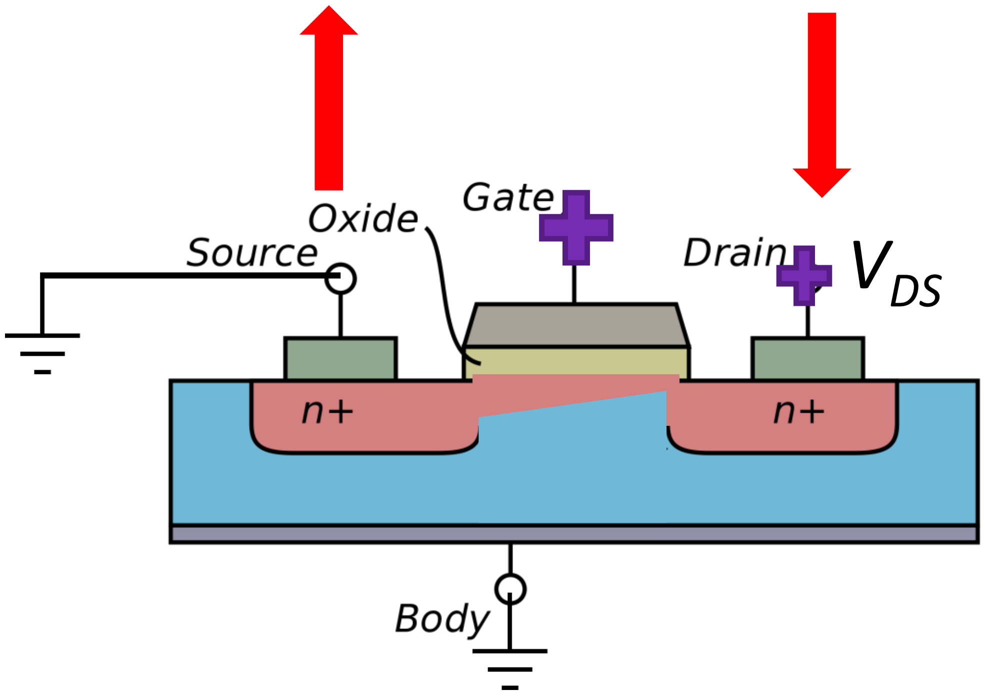


Creating a channel





Creating a channel



$V_G > V_t$

$V_{DS} < V_G - V_t$

- If $V_G > V_t$ and $0 \leq V_{DS} \leq V_G - V_t \equiv V_{OD}$
- V_G controls the Area of the channel
- FET acts as a variable resistor
- The conductance drain to source is

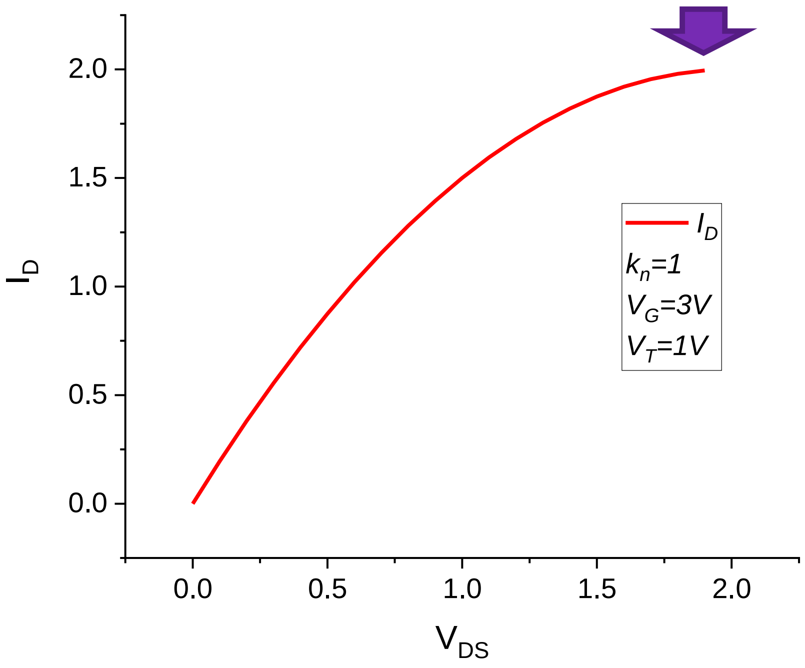
$$g_{DS} = \frac{1}{R_{DS}} = k_n \left(V_G - V_t - \frac{1}{2} V_{DS} \right)$$

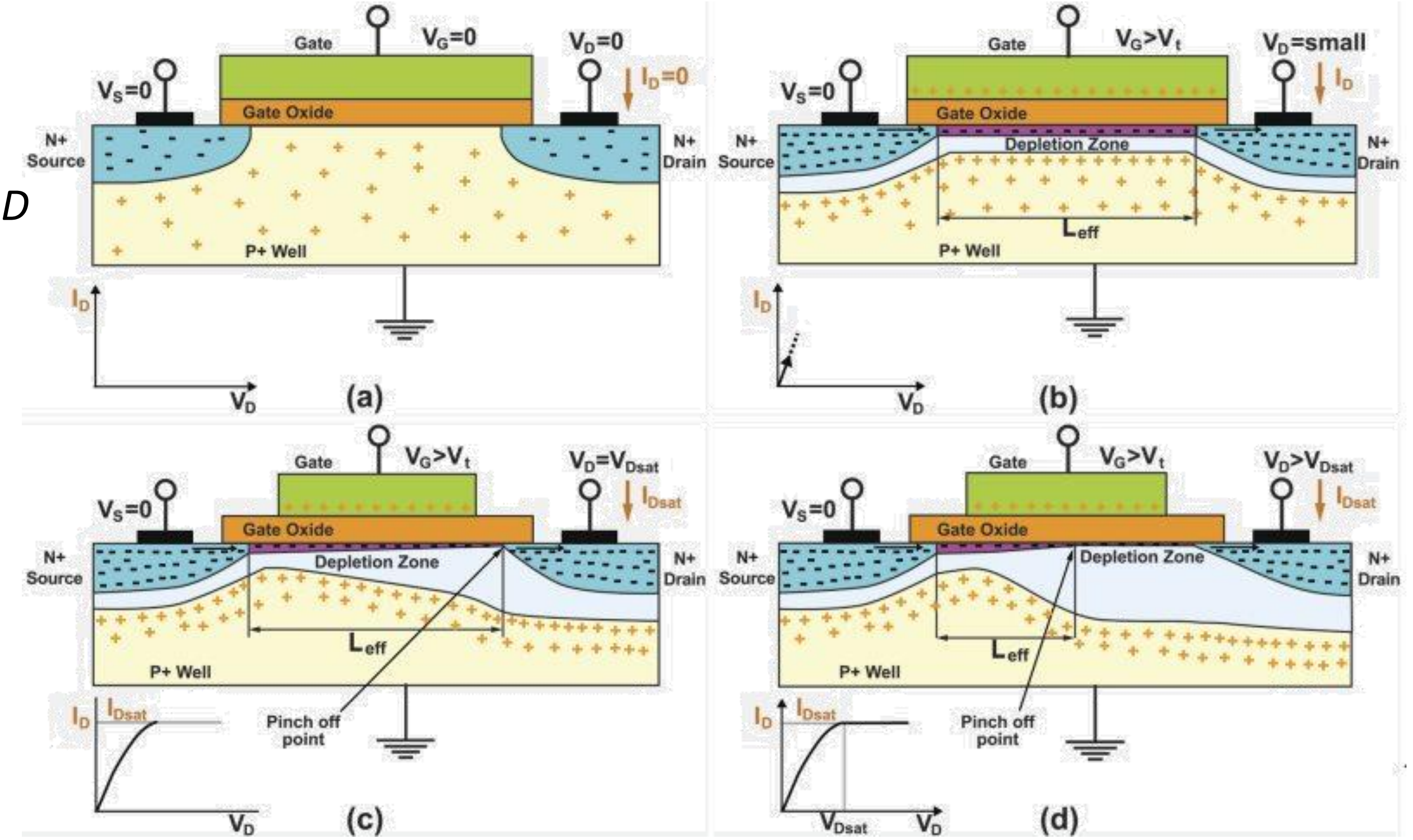
- And the current drain to source is

$$I_D = k_n \left(V_G - V_t - \frac{1}{2} V_{DS} \right) V_{DS}$$

Variable resistor

$$V_{DS} = V_G - V_t \equiv V_{OD}$$





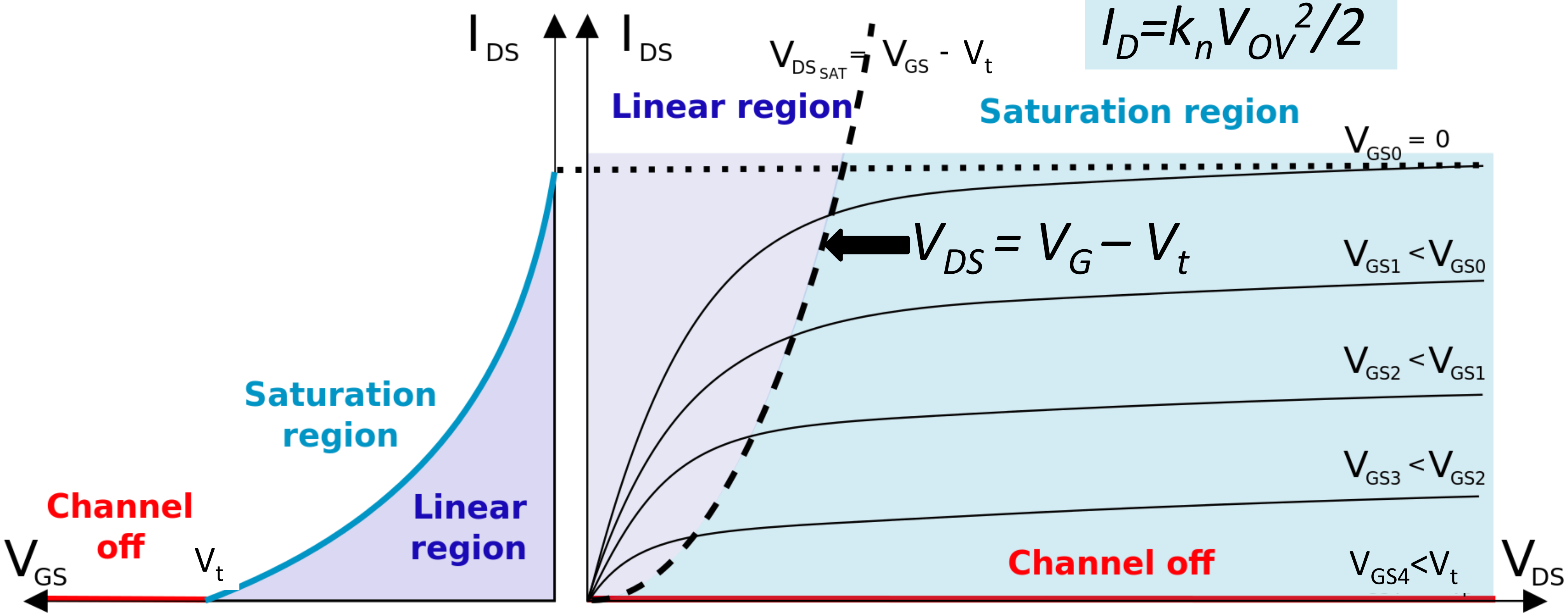
https://www.mks.com/n/mosfet-physics

Operation modes, output characteristics

$V_{DS} \leq V_G - V_t$

$V_{DS} \geq V_G - V_t$

$I_D = k_n V_{OV}^2/2$

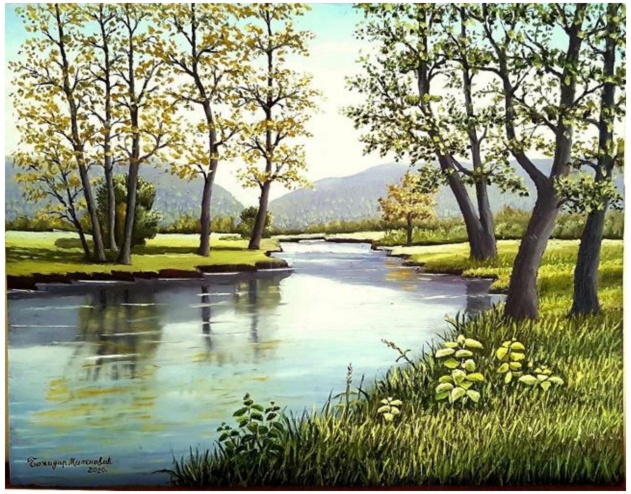


$V_{GS} \leq V_t$

What is k_n?

Mobility

- How easy is for current carriers to move in the channel?



“High mobility”

“Low mobility”

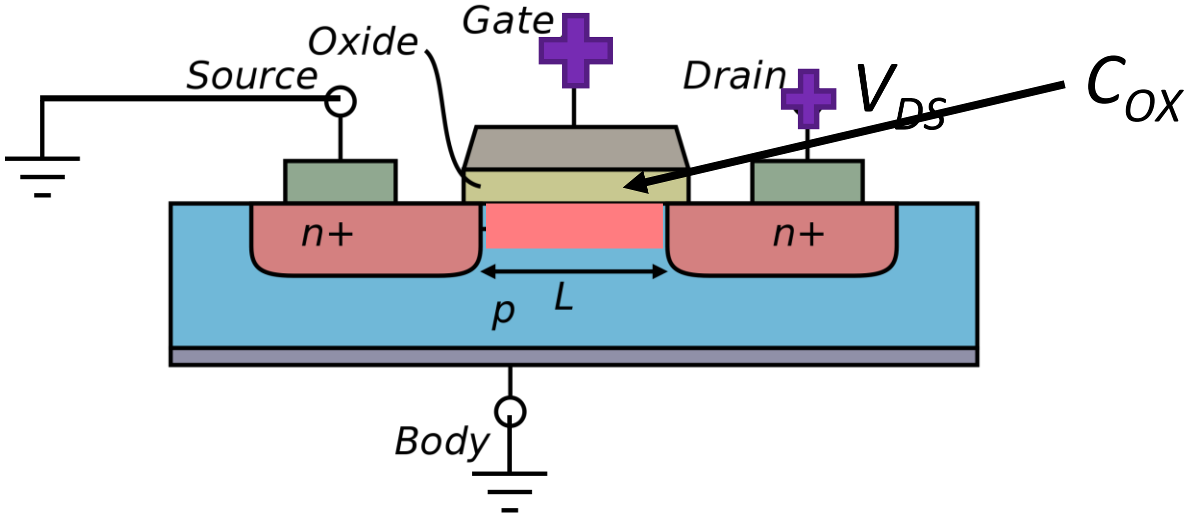
- Less obstacles – higher mobility (μ), higher k_n

$$k_n \propto \mu$$

What is k_n?

Capacitance

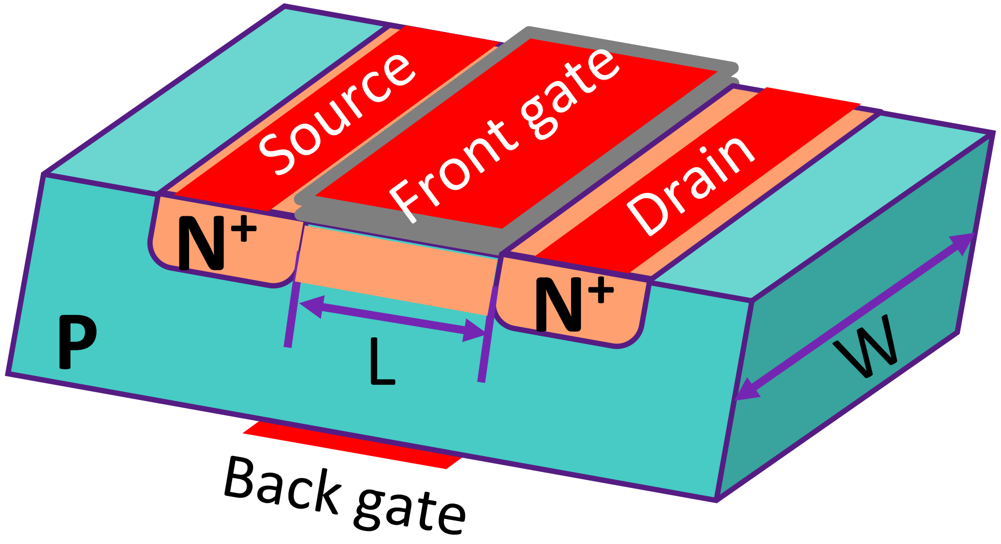
$V_G > V_t \qquad V_{DS} \leq V_G - V_t$



- Larger C_{OX}, more charge carriers can enter the channel for the same V_G.

$$k_n \propto C_{OX}$$

Aspect ratio



- Larger *W* – more carriers enter the channel. Smaller *L* faster and “more successfully” they pass it.

$$k_n \propto W/L$$

What is k_n?

$$\boldsymbol{k_n = \mu C_{OX}\frac{W}{L}}$$

Units are A/V²

So, current is simply

$$I_D = \mu C_{OX}\frac{W}{L}\left(V_G - V_t - \frac{1}{2}V_{DS}\right)V_{DS}$$

But in the next presentation…

$$I_D = u_T\mu_0 Q_i\frac{W_{CH}}{L_{CH}}\left[1 - exp\left(\frac{-V_{DS}}{u_T}\right)\right] \xleftrightarrow[\text{INV}]{\text{STS}} I_D = \mu_n Q_i\frac{W_{CH}}{L_{CH}}V_{DS}$$

$$Q_i(V_g) = C_{FOX} n u_T LW\left(e^{\frac{V_g - V_{th}}{n u_T}}\right)$$

$$\mu_n = \frac{\mu_0}{1 + \theta_1(Q_i/C_{FOX}) + \theta_2(Q_i/C_{FOX})^2}$$

$u_T = k_B T/q$, k_B- Boltzmann's constant
T – temperature, q - elementary charge
μ_n , μ_0 – electron and low field mobility
W_{CH}, L_{CH} the gate width and length
Q_i - inversion charge
V_t - threshold voltage
C_{FOX} front oxide capacitance
Bias: V_g – gate, V_{DS} drain-source
n - quality factor (n=STS_{meas}/STS_{th}),
"*LW*" stands for Lambert W function.
θ_1, θ_2 mobility attenuation coefficients

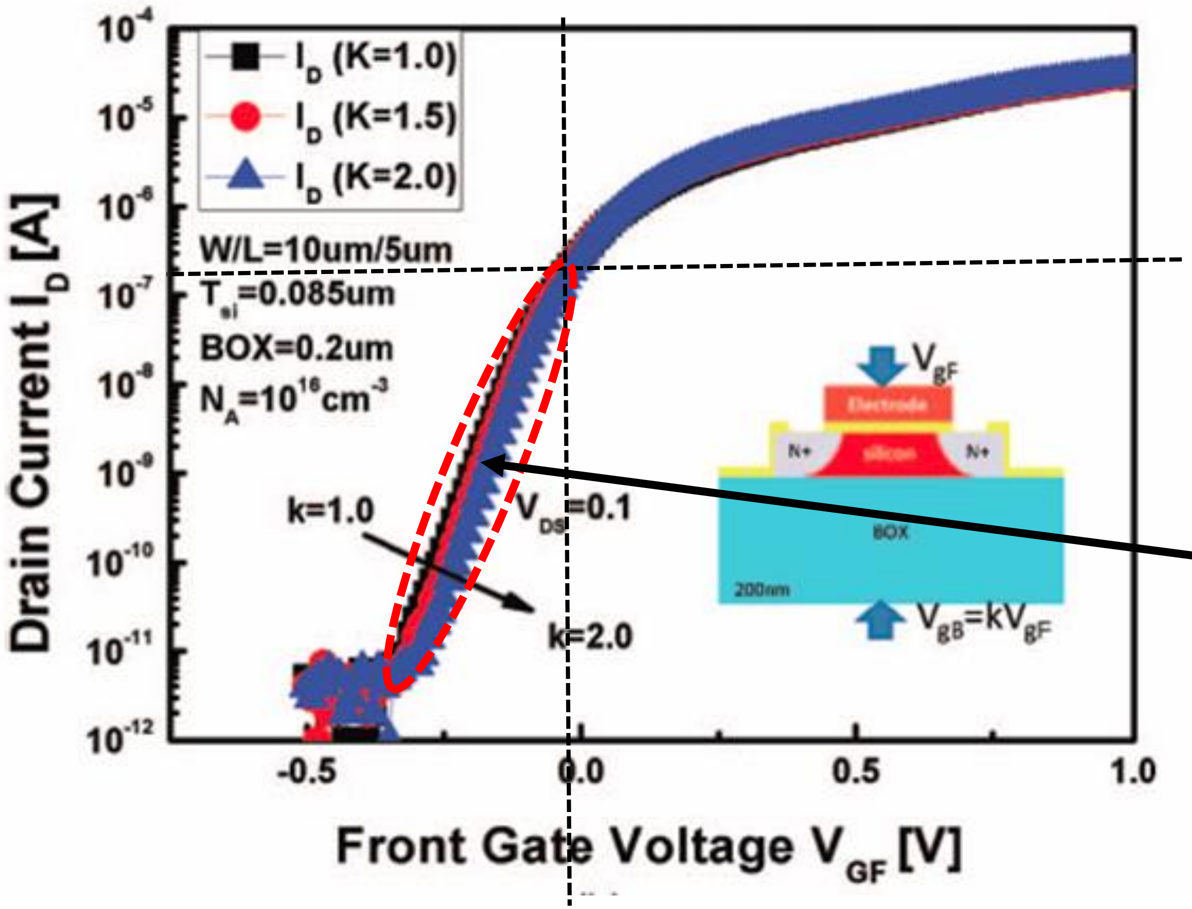
What are all these parameters?

$u_T = k_B T/q$, k_B- Boltzmann’s constant
T – temperature, q - elementary charge
μ_n , μ_0 – electron and low field mobility
W_{CH}, L_{CH} the gate width and length
Q_i - inversion charge
V_t - threshold voltage
C_{FOX} front oxide capacitance
Bias: V_g – gate, V_{DS} drain-source
$n(\eta)$ - quality factor ($n = STS_{meas}/STS_{th}$),
“*LW*“ stands for Lambert W function.
θ_1, θ_2 mobility attenuation coefficients

S. Remillard (2022), Lectures 71,72
M. Lundstrom, “Fundamentals of Nanotransistors”, World Sci, (2018)

Subthreshold current

J.-Y. Cheng et al. ECS Sol. St. Lett. 2013, **2**, Q32



$0.1W/L\ (\mu A)$

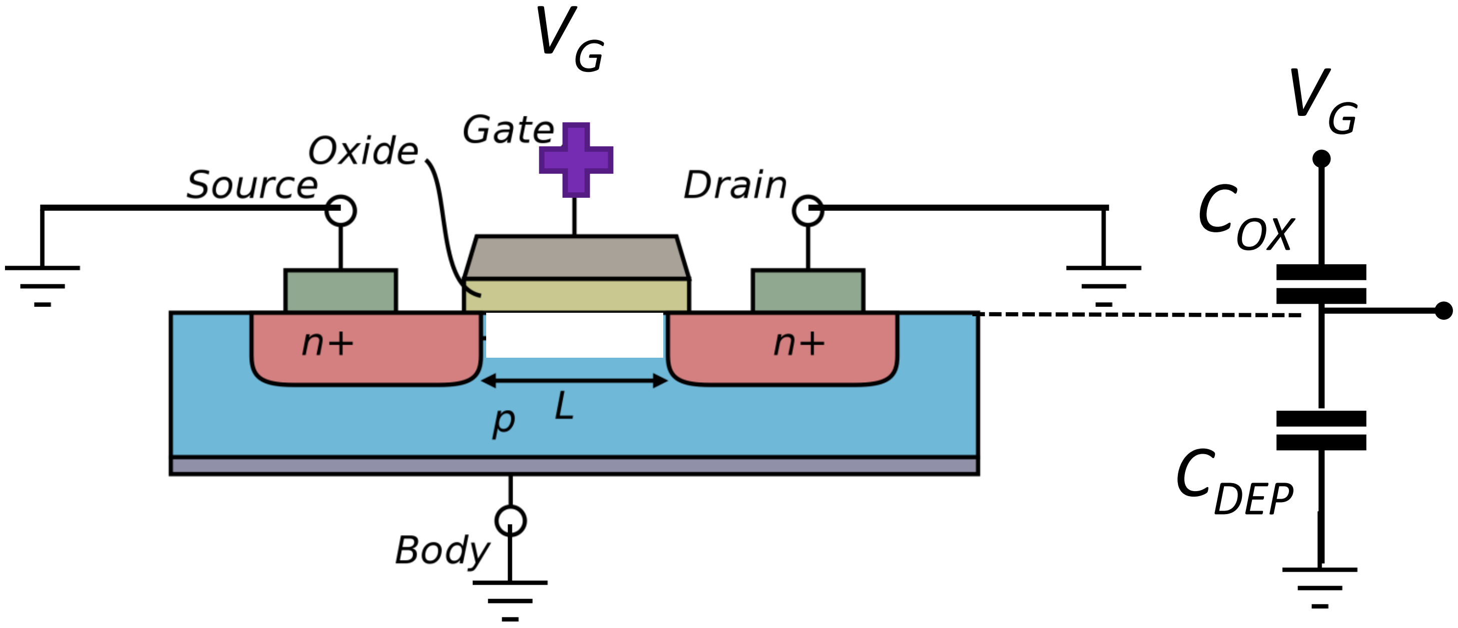
V_t

$$Slope = \frac{d(logI_D)}{dV_G} = \frac{1}{STS}$$

Larger slope (smaller STS≡SS)
→ smaller V_{OFF} - V_t(good!)

IV for subthreshold range

Depletion (!)



Surface potential:

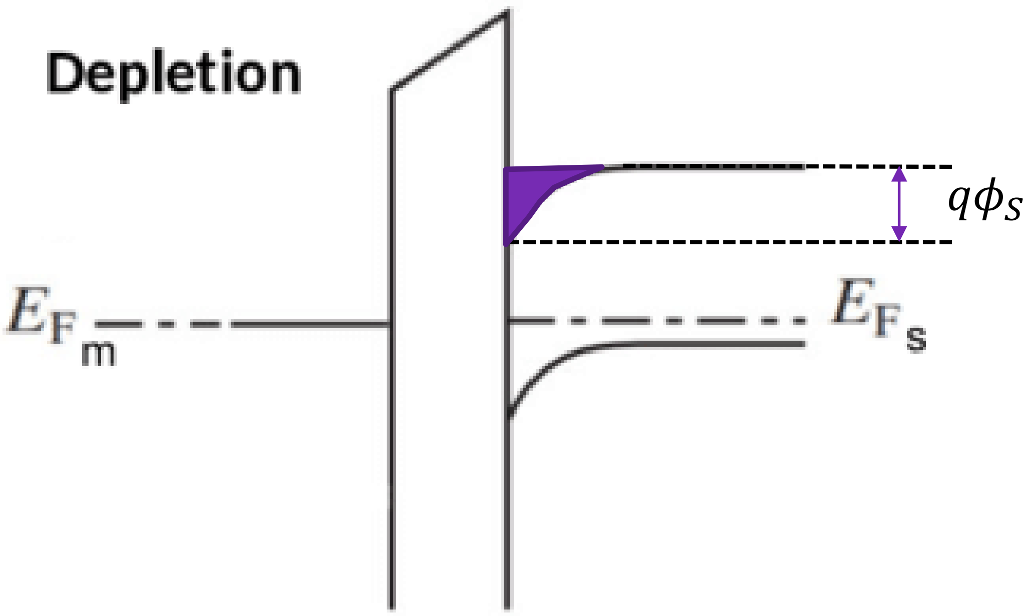
$$\phi_S = V_G \frac{C_{OX}}{C_{OX} + C_{DEP}}$$

$$\frac{d\phi_S}{dV_G} = \frac{C_{OX}}{C_{OX} + C_{DEP}} = \frac{1}{\eta}$$

$$\eta = 1 + \frac{C_{DEP}}{C_{OX}}$$

$$\eta \equiv n$$

Drain-source current



$$\frac{d\phi_S}{dV_G} = \frac{1}{\eta} \rightarrow \phi_S = \int_{V_{fb}}^{V_G} \frac{1}{\eta} dV'_G = \frac{V_G}{\eta} - \frac{V_{fb}}{\eta}$$

Density of electrons:

$$n_S = N_C \exp \frac{[E_F - (E_C - q\phi_S)]}{kT}$$

$$n_S = \boxed{N_C \exp \frac{(E_F - E_C)}{kT}} \exp\left(\frac{q\phi_S}{kT}\right)$$

$$n_S = \boxed{n_{bulk}} \exp\left(\frac{q\phi_S}{kT}\right)$$

$$n_S = \left[n_{bulk} \exp\left(\frac{-qV_{fb}}{\eta kT}\right)\right] \exp\left(\frac{qV_G}{\eta kT}\right)$$

Drain-source current

$$I_D = AQ_n v = W(qn_S D)v$$

$$I_D = \left[qvn_{bulk}\exp\left(\frac{-qV_{fb}}{\eta kT}\right)DW\right]\exp\left(\frac{qV_G}{\eta kT}\right) = B\exp\left(\frac{qV_G}{\eta kT}\right)$$

! When V_G=V_t the current I_D=0.1(W/L) µA $\rightarrow 0.1\frac{W}{L} = B\exp\left(\frac{qV_t}{\eta kT}\right)$

$$B = 0.1\frac{W}{L}\exp\left(-\frac{qV_t}{\eta kT}\right) \quad \rightarrow \quad I_D = 0.1\frac{W}{L}\exp\left[\frac{q(V_G - V_t)}{\eta kT}\right]$$

Question for the students: Which voltage is absent in this nice equation?

No V_{DS} in the expression for I_D?!

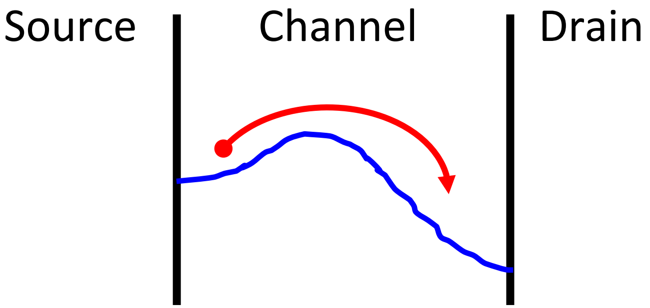
What happened to V_{DS}?

$$I_D = u_T \mu_0 Q_i \frac{W_{CH}}{L_{CH}} \left[1 - exp\left(\frac{-V_{DS}}{u_T} \right) \right]$$

$$Q_i(V_g) = C_{FOX} \eta u_T LW (e^{\frac{V_g - V_{th}}{\eta u_T}})$$

At 300K, u_T=$k_B T/q$ = 25.85 mV, the "thermal voltage".

Usually, $V_{DS} >> \frac{k_B T}{q}$ and $exp\left(\frac{-qV_{DS}}{k_B T}\right) \approx 0$



📖 M. Lundstrom, “Fundamentals of Nanotransistors”, World Sci, (2018)

Drain-source current below V_t

- There is **no continuous flow** (drift current) of electrons in the channel volume below threshold.
- Carriers flow by **thermionic emission**: imagine the channel as a potential barrier and a carrier crossing this barrier if it gets enough energy from the lattice at given temperature.

What is LW and why it appears for FD SOI?

The Lambert W(x) function is defined as the inverse function of

$$y \exp y = x$$

the solution being given by

$$y = W(x)$$

or shortly

$$W(x) \exp W(x) = x$$

D: [-1/e, ∞); R: [-1, ∞)

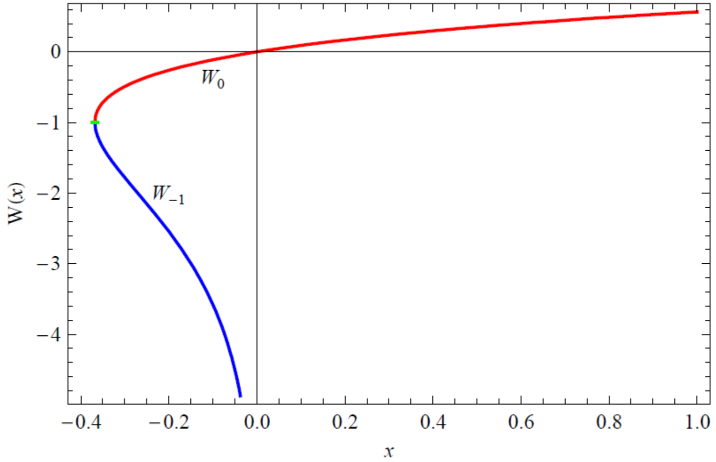


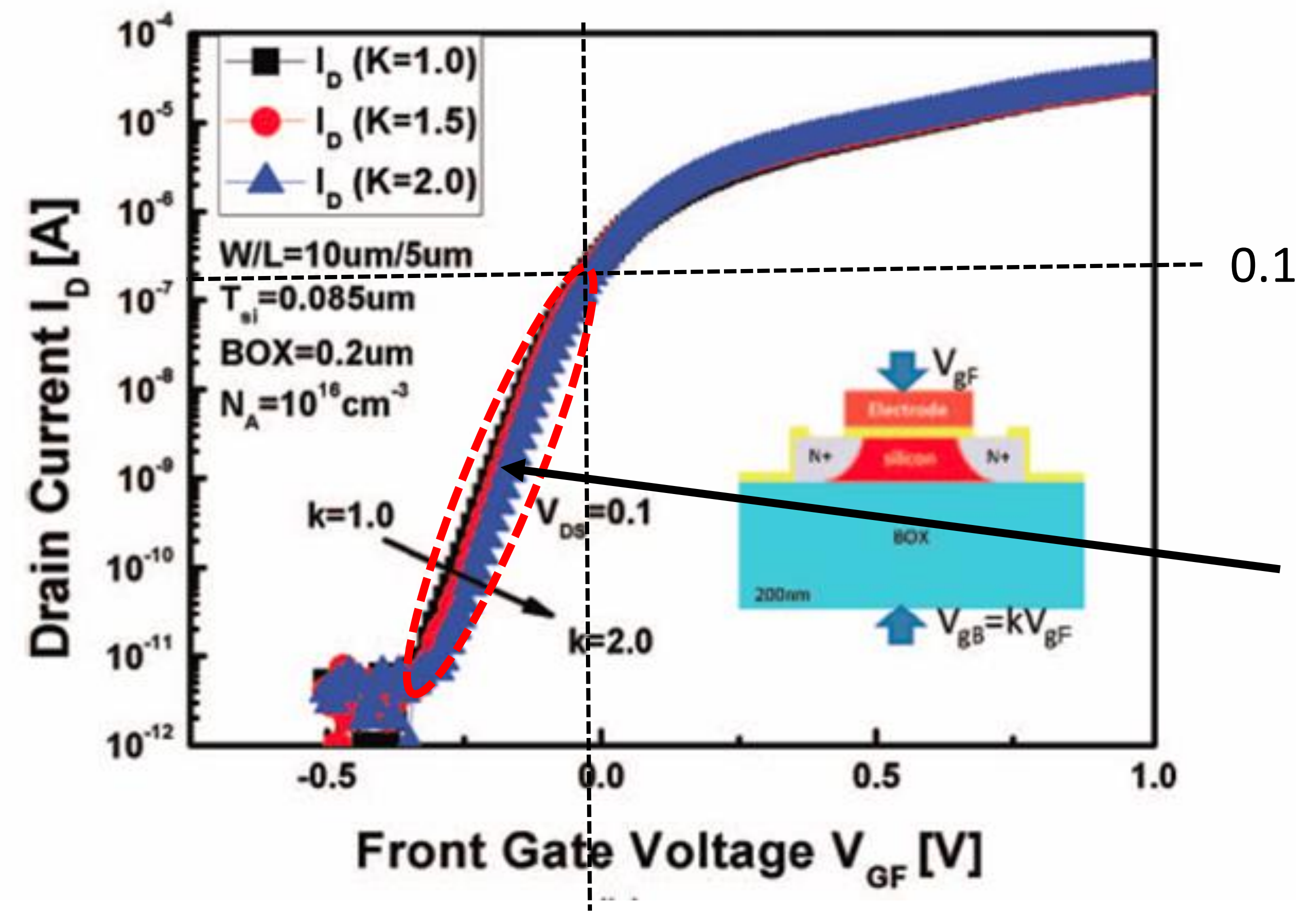
Figure 1: The two branches of the Lambert W function, $W_{-1}(x)$ in blue and $W_0(x)$ in red. The branching point at $(-e^{-1}, -1)$ is denoted with a green dash.

D. Veberic, arXiv:1003.1628v2 [cs.MS] 7 Jan 2018

T.A. Karatsori, et al., Sol.-St. Electron., 2015, **111**, 123

So, what about subthreshold swing?

J.-Y. Cheng et al. ECS Sol. St. Lett. 2013, **2**, Q32



$0.1W/L\ (\mu A)$

V_t

$$Slope = \frac{d(logI_D)}{dV_G} = \frac{1}{STS}$$

Larger slope (smaller STS)
→ smaller V_{OFF} - V_t(good!)

So what about subthreshold swing?

$$I_D = 0.1\frac{W}{L}\exp\left[\frac{q(V_G - V_t)}{\eta kT}\right] \equiv 0.1\frac{W}{L}\exp\left[\frac{-qV_t}{\eta kT}\right]\cdot\exp\left[\frac{qV_G}{\eta kT}\right]$$

At RT (295K):

V_G	$\exp\left[\frac{qV_G}{\eta kT}\right] = \exp\left[\frac{V_G}{\eta * 0.026}\right]$
(100 mV)*η	Calculate!
(160 mV)*η	
(220 mV)*η	
(280 mV)*η	
Δ=60 mV	

$$\ln(I_D) = \ln\left\{0.1\frac{W}{L}\exp\left[\frac{q(V_G - V_t)}{\eta kT}\right]\right\}$$

$$\frac{d\ln(I_D)}{dV_G} = \frac{q}{\eta kT} = \frac{1}{(0.026\,V)\eta}$$

$$\ln(I_D) = 2.3\log(I_D)$$

$$\frac{d\log(I_D)}{dV_G} = \frac{q}{2.3\eta kT} = \frac{1}{STS}$$

At RT for every 60 mV change in V_G, I_D changes 10 times!

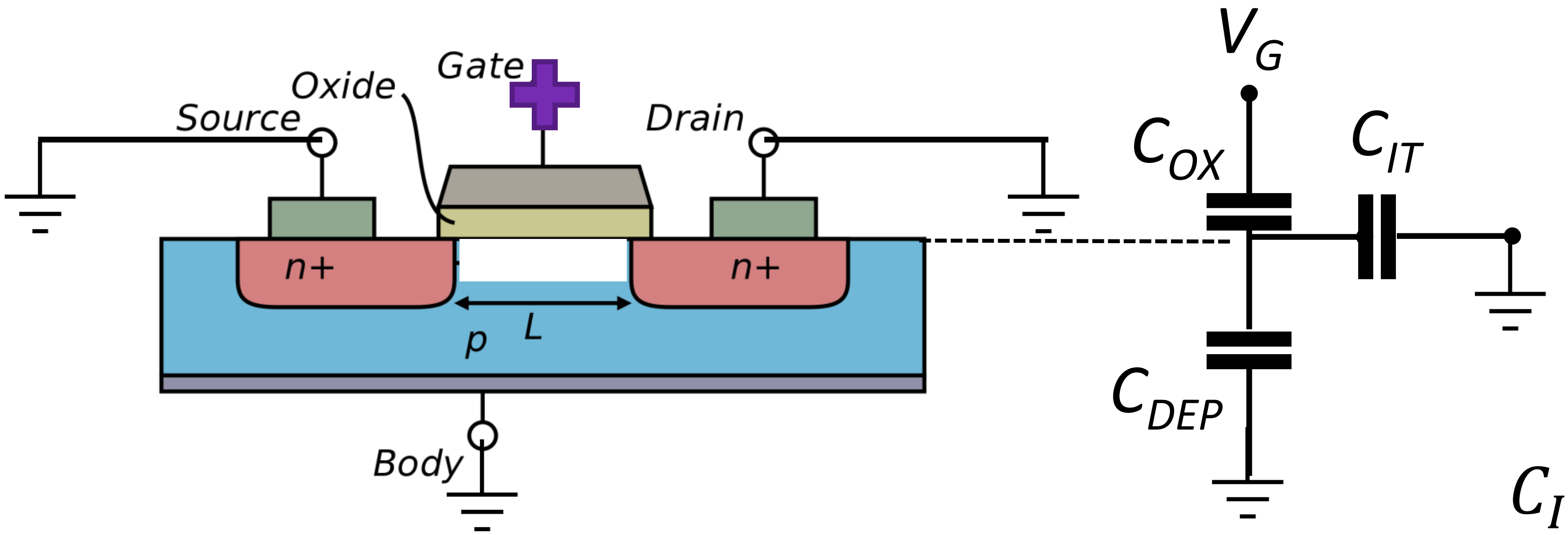
$$\frac{d\log(I_D)}{dV_G} \approx \frac{1}{60\,mV\cdot\eta}$$

$STS_{TH,\mathrm{RT}} \approx$ **60 mV**

$$\eta = 1$$

Subthreshold swing

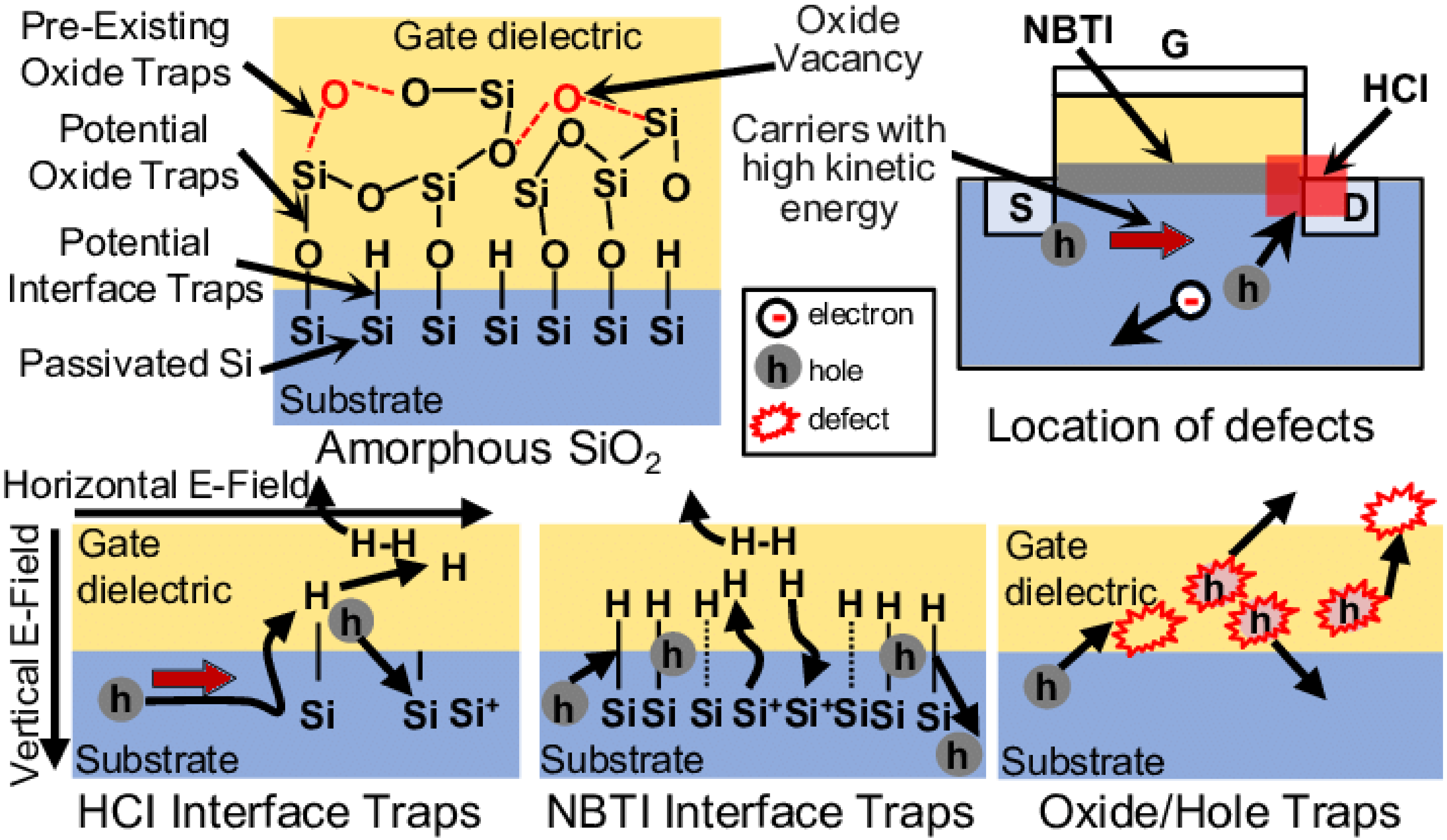
$$\frac{d\log(I_D)}{dV_G} = \frac{q}{2.3\eta kT} = \frac{1}{STS} \quad \rightarrow \quad STS = \frac{2.3\eta kT}{q} \; ; \quad \eta = 1 + \frac{C_{DEP}}{C_{OX}} \; ; \quad \frac{C_{DEP}}{C_{OX}} \ll 1 \text{ and } \eta \geq 1$$



$$\eta = 1 + \frac{C_{DEP} + C_{IT}}{C_{OX}}$$

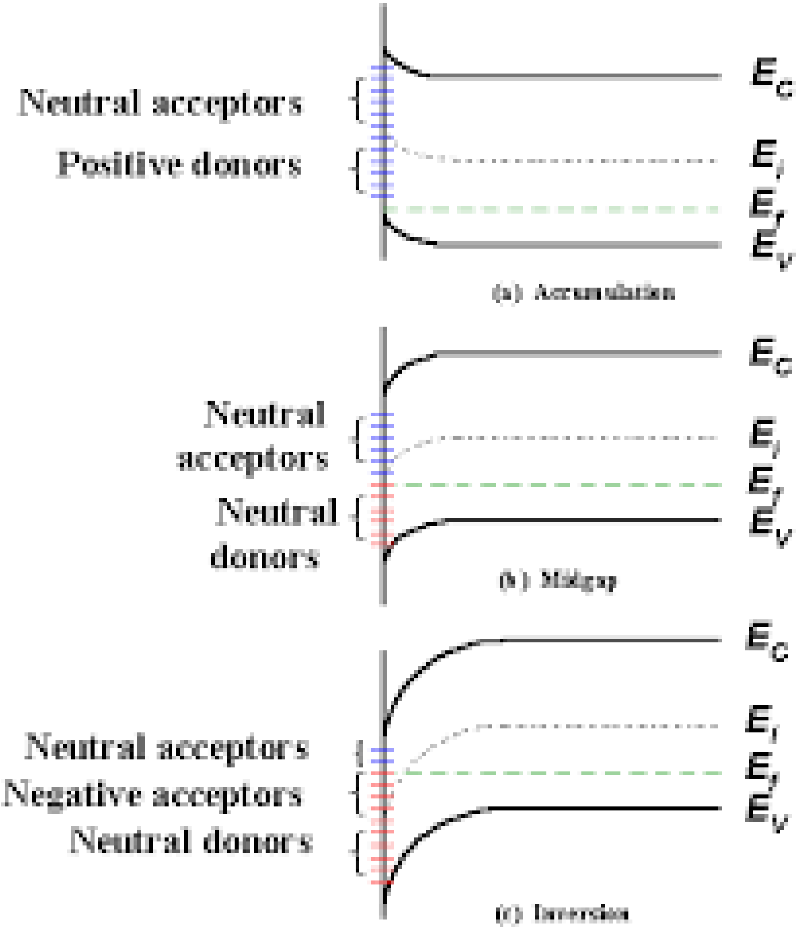
C_{IT} is related to interface traps: $C_{IT} = qD_{IT}$

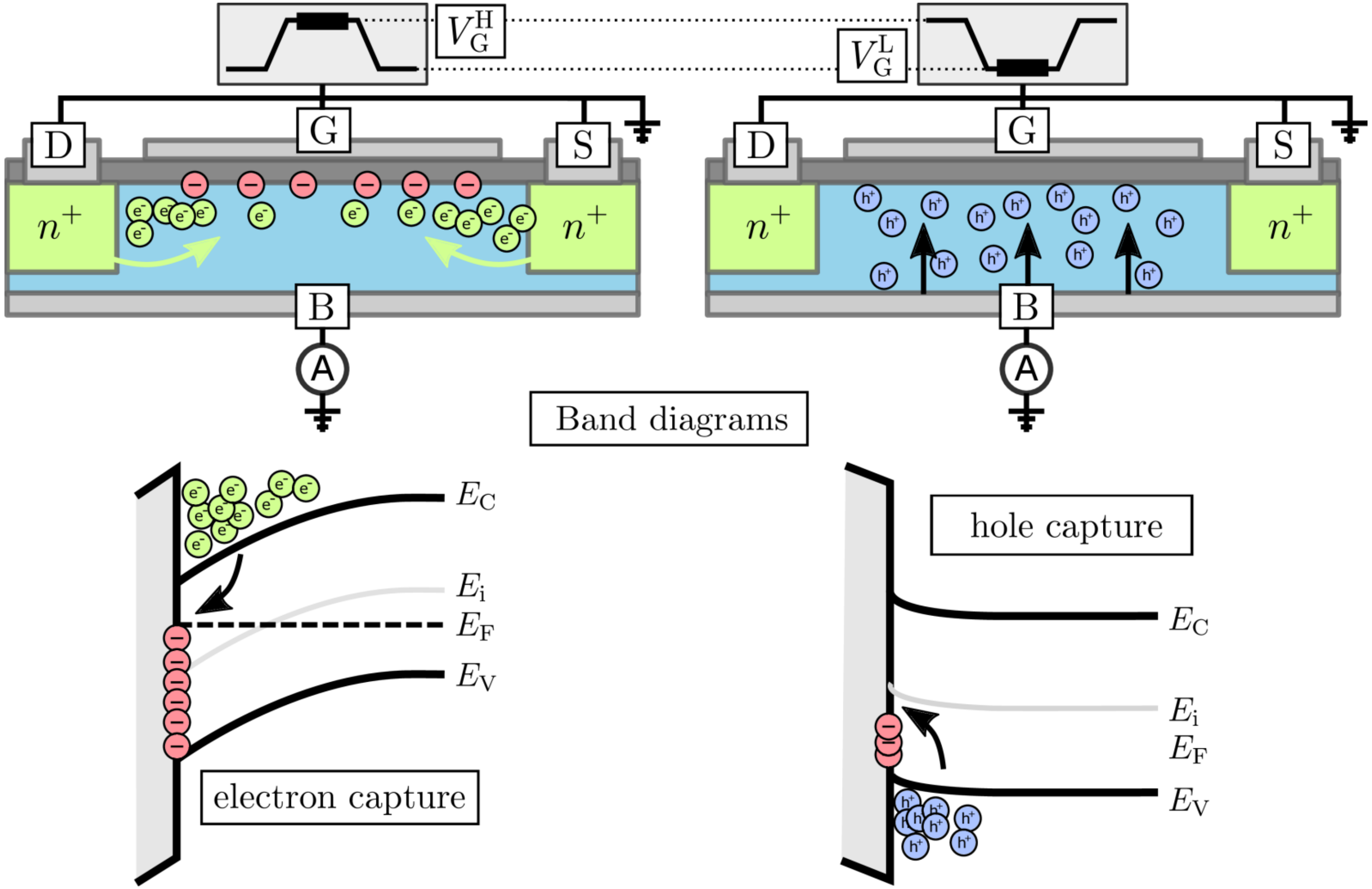
Interface traps



J. Lienig, et al., ICCAD 20121 DOI: 10.1109/ICCAD51958.2021.9643447

Influence of interface traps on MOSFET





https://www.iue.tuwien.ac.at/phd/rescher/Methodology.html

Summary: what was considered

- ✓ **FD SOI**
- ✓ **HKMG Stack**
- ✓ **MOSFET, $I_d V_g$, V_{th} and STS (SS, S)**
- ✓ **Carrier mobility**
- ✓ **Interface traps**

IAP

TECHNISCHE UNIVERSITÄT
BERGAKADEMIE FREIBERG
Die Ressourcenuniversität. Seit 1765.

Thank you for attention!

International School and Conference on Functional Materials for Modern Technologies

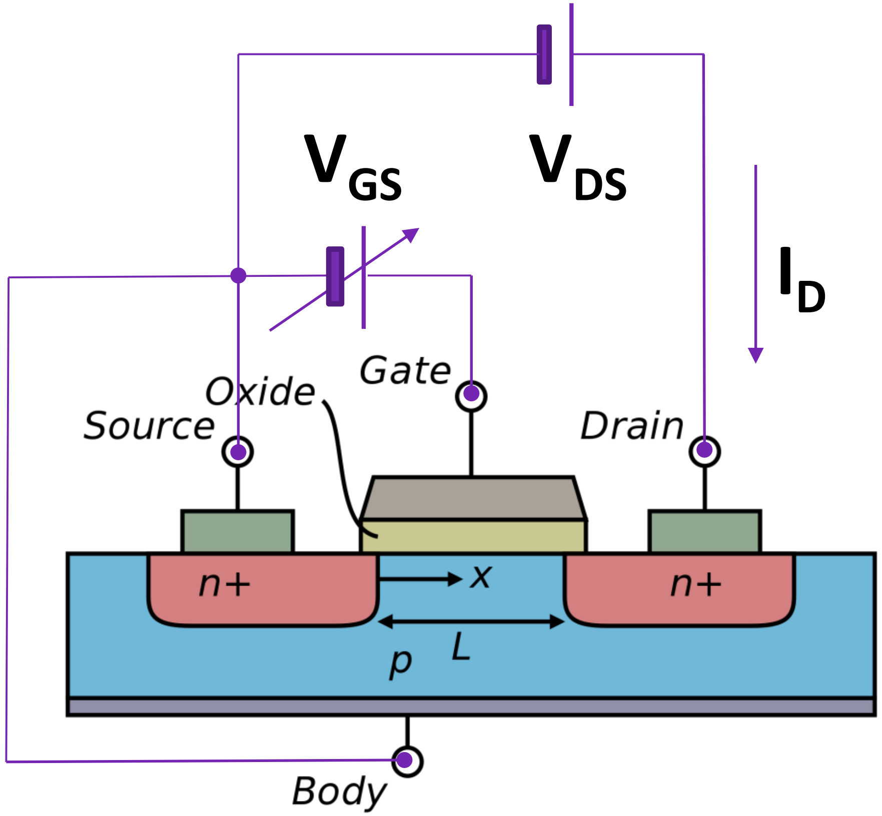
ISCFMMT 2022

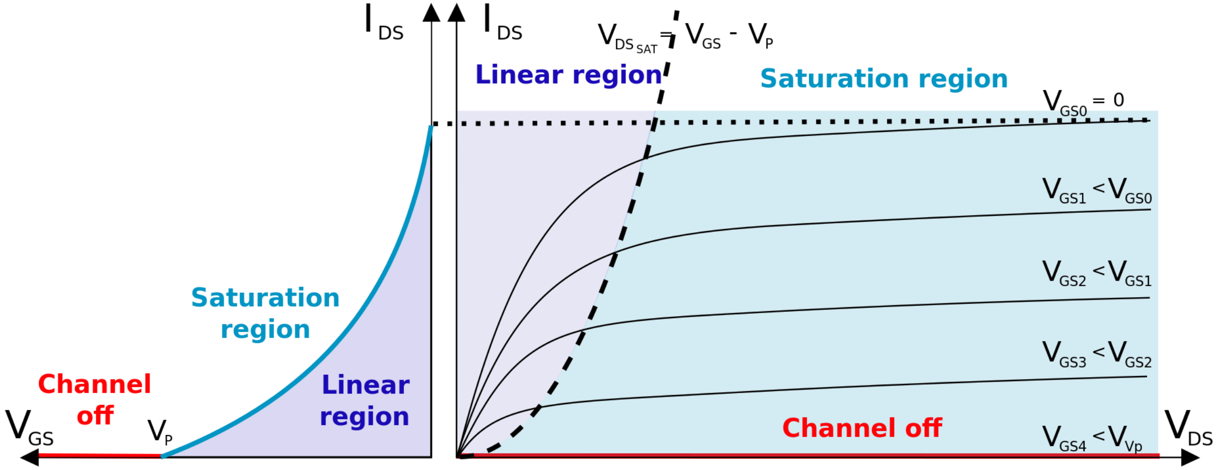
Batumi Shota Rustaveli State University, Batumi, Georgia October 1-7 2022

What to read and watch:

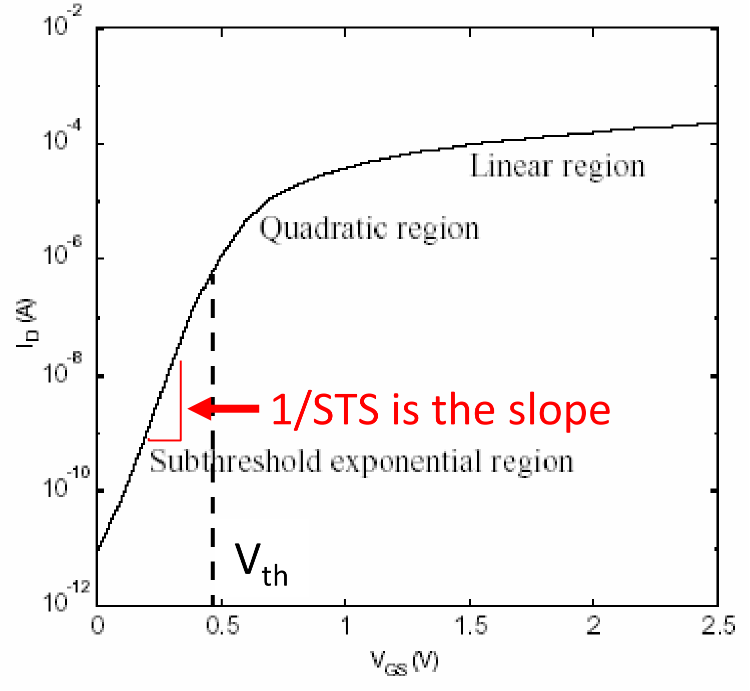
- ▶ L.R Linares and J. Yan (2013)
- 📖 A.S. Sedra and K.C. Smith, “Microelectronic Cirquits”, 6th edition (2009)
- 📖 K. Yim, et al., NPG Asia Materials, 2017, 7, 190
- 🌐 By Tech2077 - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=65081300
- 🌐 By JFET_n-channel.svg: Phirosiberiaderivative work: Phirosiberia (talk) - JFET_n-channel.svg, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=7042107
- 📖 K.H. Yeap, M.M. Isa and S. H. Loh, (2020) DOI: 10.5772/intechopen.92818
- 🌐 https://www.mks.com/n/mosfet-physics
- ▶ S. Remillard (2022), Lectures 71,72
- 📖 M. Lundstrom, “Fundamentals of Nanotransistors”, World Sci, (2018)
- 📖 J.-Y. Cheng et al. ECS Sol. St. Lett. 2013, **2**, Q32
- 📖 M. Lundstrom, “Fundamentals of Nanotransistors”, World Sci, (2018)
- 🌐 D. Veberic, arXiv:1003.1628v2 [cs.MS] 7 Jan 2018
- 📖 T.A. Karatsori, et al., Sol.-St. Electron., 2015, **111**, 123
- 📖 J. Lienig, et al., ICCAD 20121 DOI: 10.1109/ICCAD51958.2021.9643447
- 🌐 https://www.iue.tuwien.ac.at/phd/rescher/Methodology.html

I_dV_g , V_{th} and STS (SS)





I_dV_g , V_{th} and STS (SS)



Subthreshold (STS) regime: $V_{GS} < V_{th}$

$$I_D \propto exp\left(\frac{qV_{GS}}{nkT}\right)$$

$$STS = n\left(\frac{kT}{q}\right)\ln(10)$$

$$STS_{th} = \left(\frac{kT}{q}\right)\ln(10) \approx 60\ mV\,\Big|_{\mathrm{RT}}$$